restricted

# Lego (G)MB EoL functional tests

## For LEGO **mother board** and **grandmother board**

Villach, 2018-09-14



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# 1 Test Points and Connectors

Required connectors:

- X1: 691 210 910 002 (Wurth Elektronik)
  Connection: via Clamp (2 pins – power supply)?
- X3: PCN13-32S-2.54DS(71) (Hirose Electric)
  Counterpart: PCN10-32P-2.54DS(72) or PCN10-32P-2.54DSA(72) (Hirose Electric)
- X2 and X5: FTSH-105-01-L-D-RA (Samtec)
  Connection: Power board assembly (X1 and X2: FLE-105-01-G-DV (Samtec))
- X6: 690 367 181 072 (Wurth Elektronik)
  Counterpart (Cable): 690 157 001 072 connector (Wurth Elektronik) and 10-pin ribbon cable (pin spacing = 1.27mm) (e.g. 63911015521 (Wurth))
  (or PCB counterparts: 690357101072 or 690357281076 (Wurth Elektronik))

Test points used:

- GD_HO and GD_LO:
  X2 and X5 header connectors (pins 1 and 2), or unused SMD pads (from 0805 capacitors) or same net TH vias
- VS to GND connection:
  X5 header connector (pins 3 and 9), or TP5 through-hole test point pads (pins 2 and 4)
- GD_HIN and GD_LIN:
  X3 connector (pins B13 and B14), or SMT test points (round SMT 1mm diameter) TP6 and TP7
- 15V supply:
  X1 connector (pin1 – 15V, pin2 - GND), or SMD test point TP8

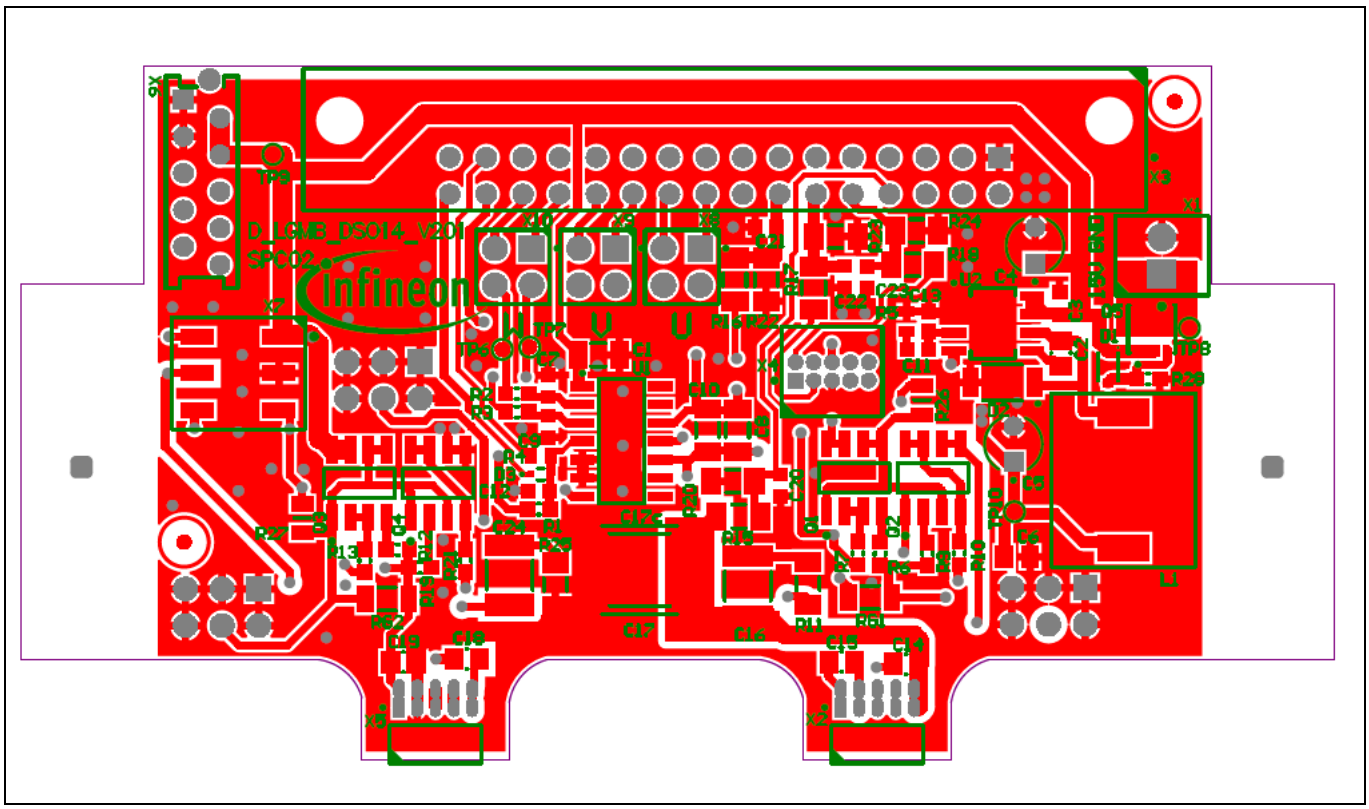



**Figure 1 PCB Print**

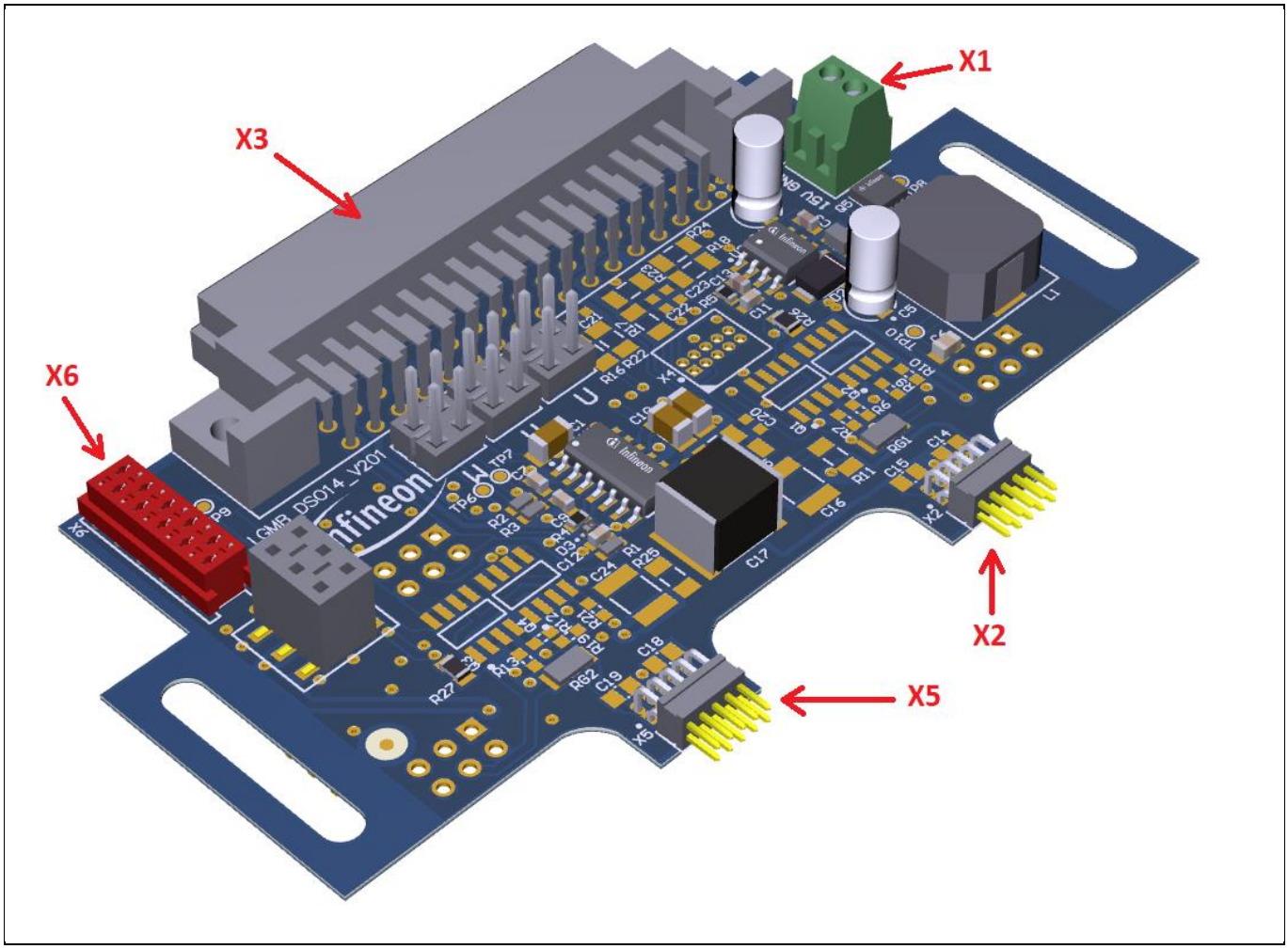



**Figure 2 Connectors on Grandmother board**

# 2 Grandmother board EoL functional test description

The objectives are:

- to test the functionality of the supply on the grandmother boards, by measuring the 5V output (at minimum load – basically only quiescent currents) while providing 15V supply at the X1 connector,
- to test the Gate driver functionality by monitoring the 2 outputs in relation to 2 provided input signals. The supply voltage from previous point is also required for this test, and in addition, it is required to short the VS node to GND_DIG1 potential.

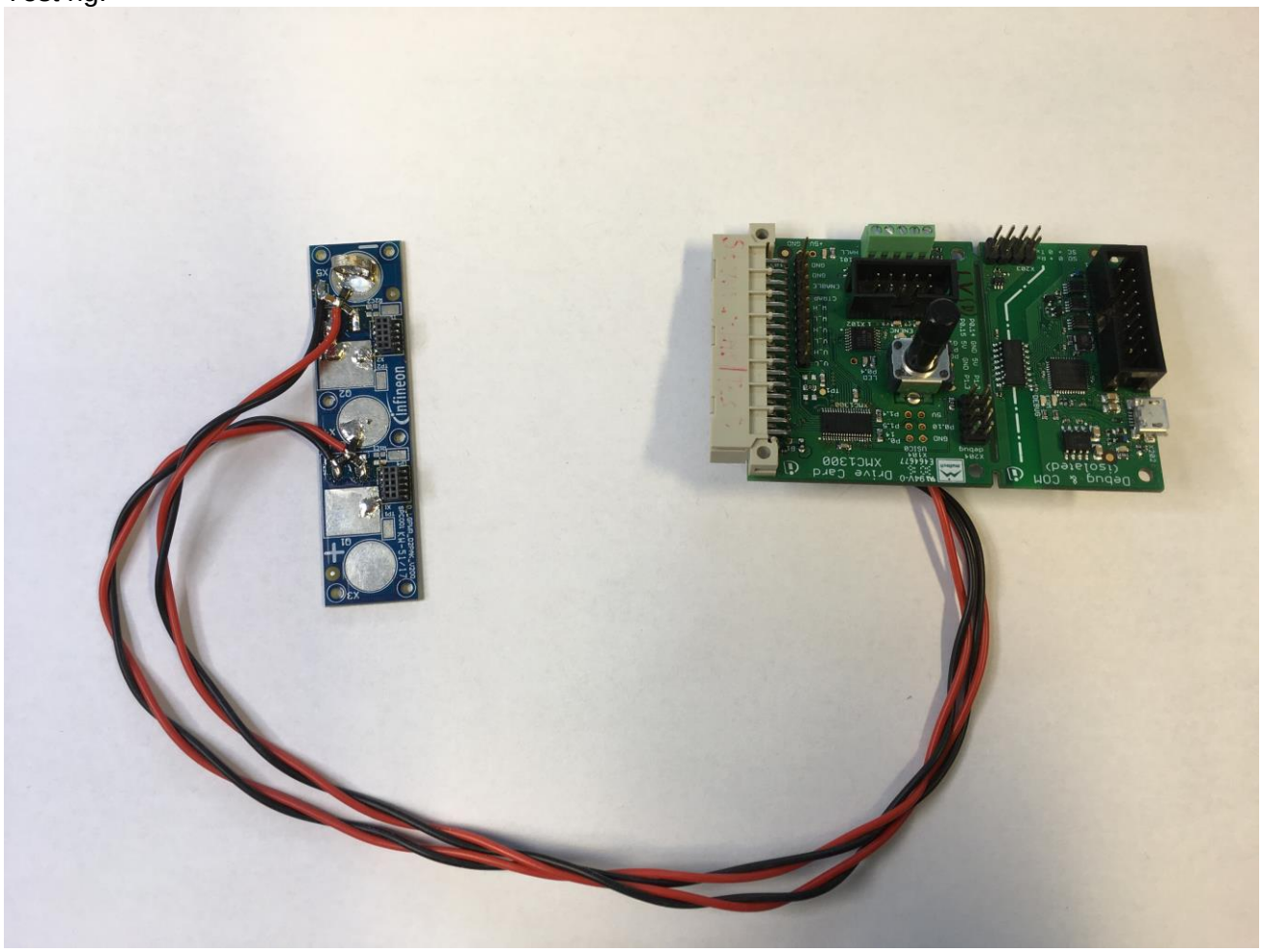
**Table 1 System inputs**

| Signal | Connection point | State | Value (tolerance) |
|---|---|---|---|
| V_Supply_X1 | X1 (pin1) | Active | 15V (±0.1V) |
| GND (reference) | X1 (pin2)<br>or<br>PWR board assembly | GND | - |
| VS to GND connection | X5 (pin9) to X5 (pin3) | Short | - |
| GD_HIN | X3 (pin B14) | High | 5V (±0.1V) |
| | | Low | 0V (±0.1V) |
| GD_LIN | X3 (pin B13) | High | 5V (±0.1V) |
| | | Low | 0V (±0.1V) |

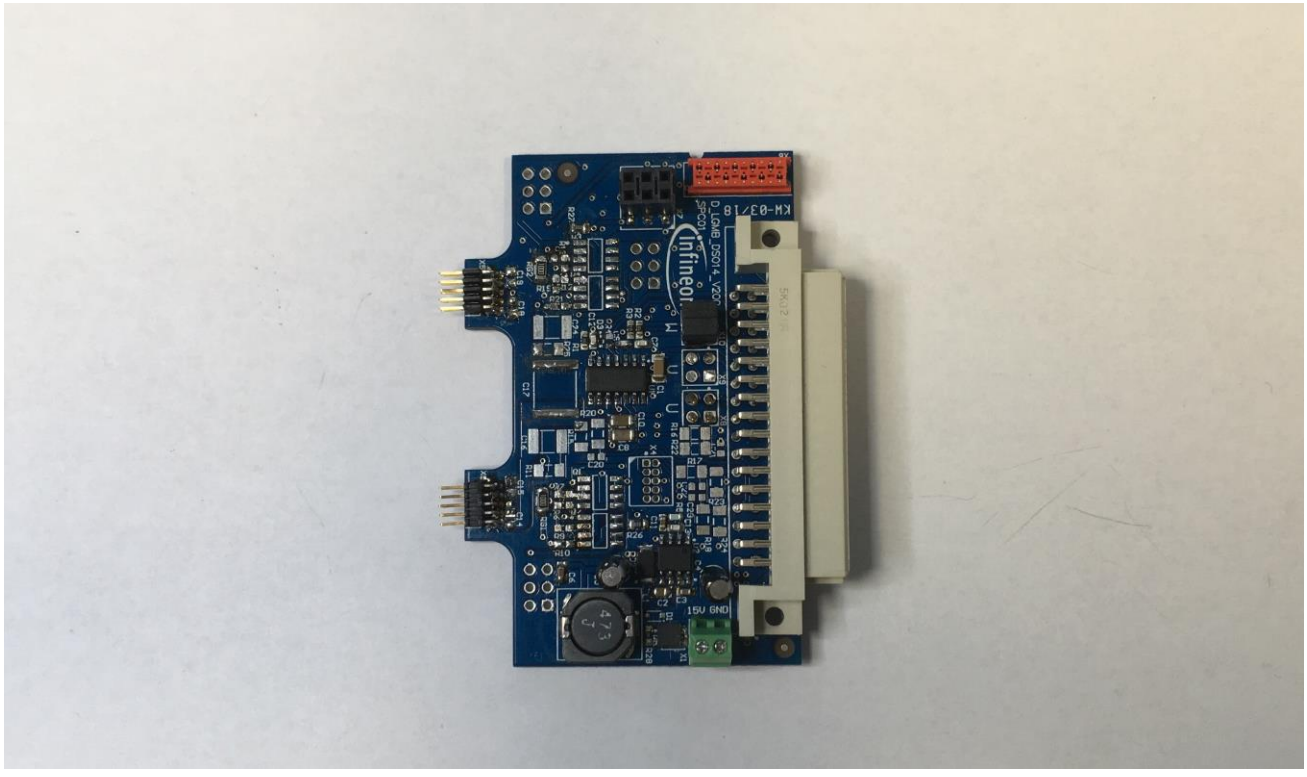
**Table 2 Measured Values (vs. GND)**

| Signal | Connection point | Dependency | Acceptance Criteria |
|---|---|---|---|
| V_DC_5V | X3 (pin B1) | V_Supply_X1 | 5V (± 0.3V) |
| GD_HO | X2 (pin 1 and 2) | GD_HIN – High | 15V (±3V) |
| | | GD_HIN – Low | 0V (±1.5V) |
| GD_LO | X5 (pin 1 and 2) | GD_LIN – High | 15V (±1.5V) |
| | | GD_LIN – Low | 0V (±1.5V) |

Test rig:

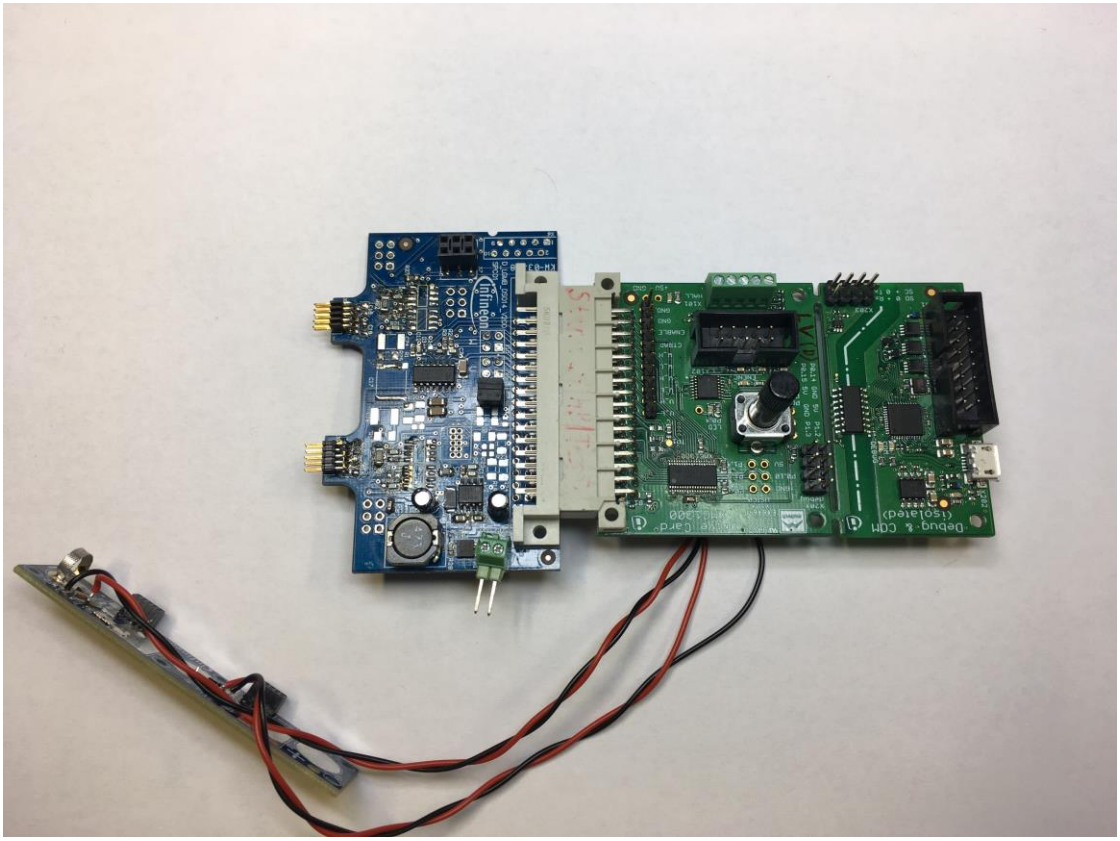


Device under test:

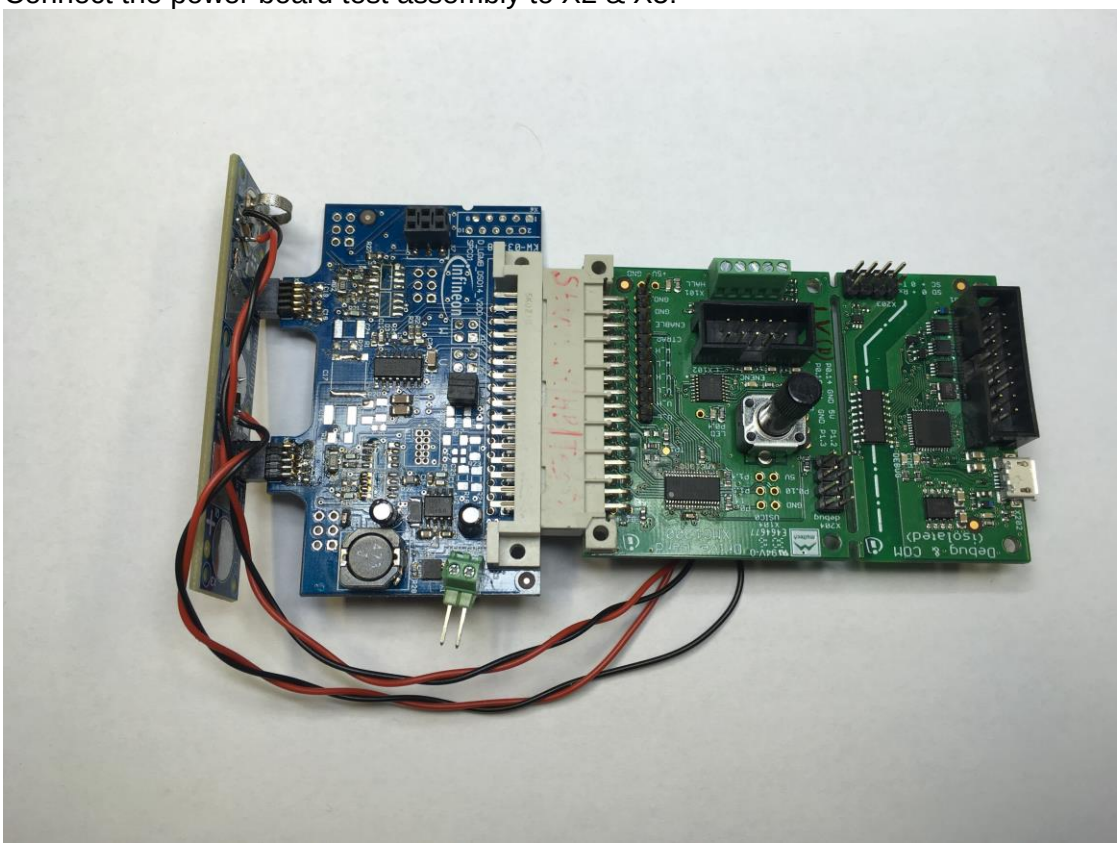


Test procedure:

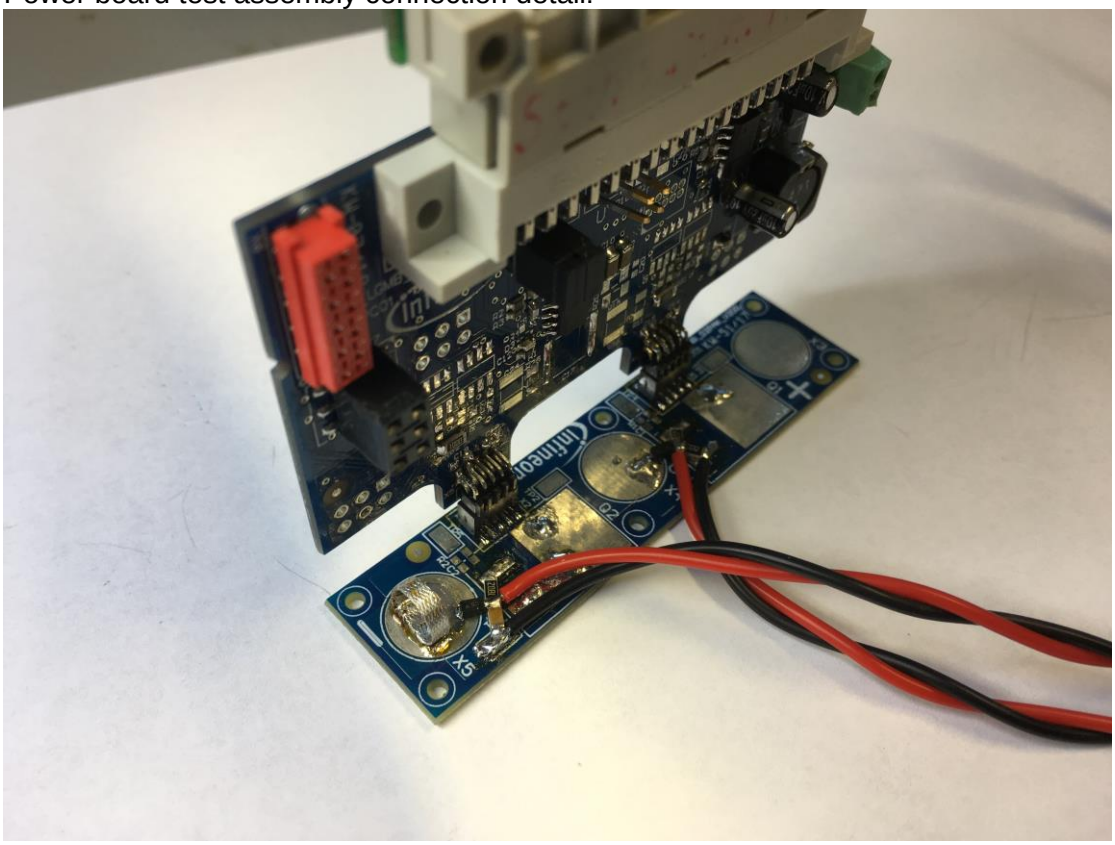
- Connect the counter connector to X3:



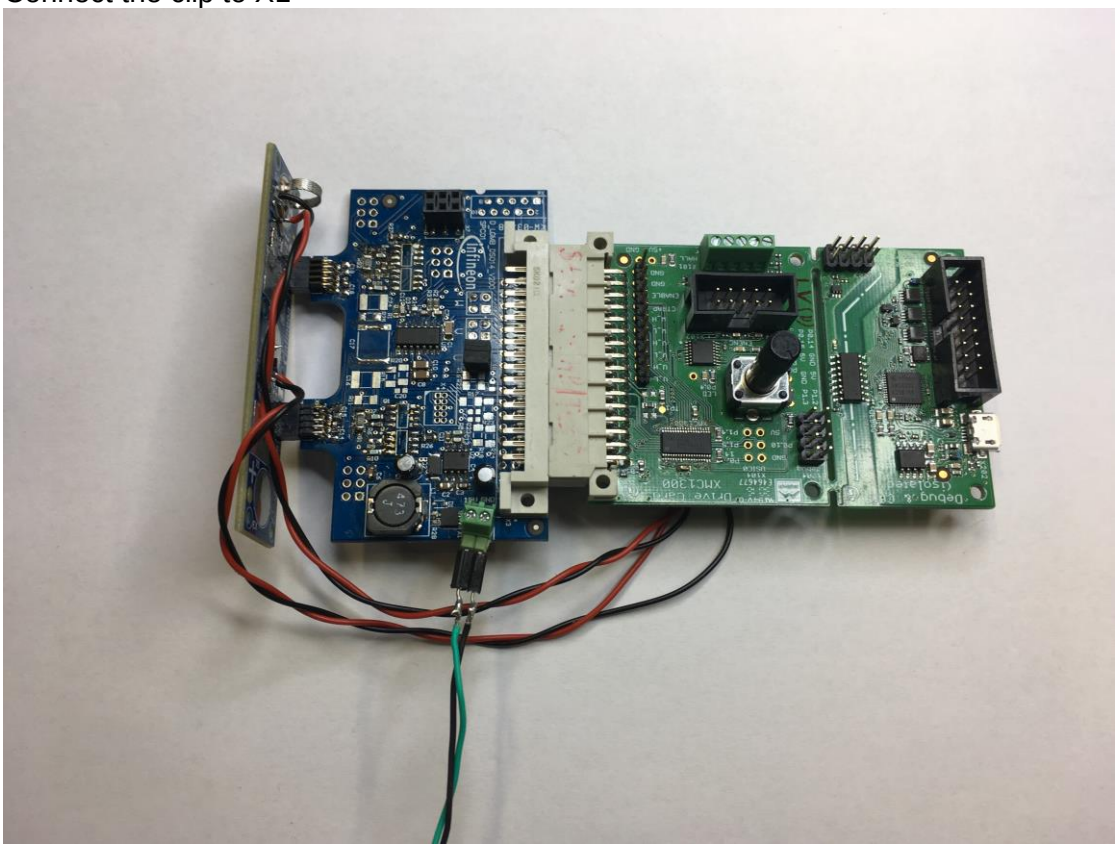
- Connect the power board test assembly to X2 & X5:



- Power board test assembly connection detail:

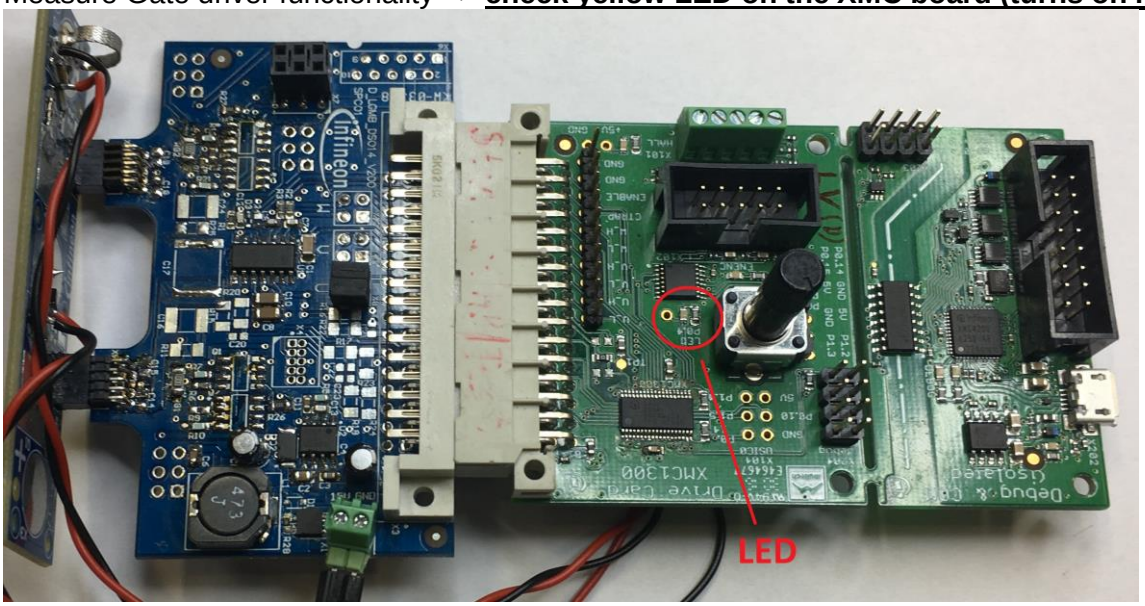


- Connect the clip to X1



- Measure V_DC_5V (X3 (pin B1) vs GND)

- Measure Gate driver functionality => **check yellow LED on the XMC board (turns on if OK)**:




**or**:
- Measure GD_HO and GD_LO @ input state 1 (GD_HIN = LOW, GD_LIN = HIGH)
- Change input state 1 >> 2)
- Measure GD_HO and GD_LO @ input state 2 (GD_HIN = HIGH, GD_LIN = LOW)

# 3 Mother board EoL functional test description

The objective is:

- to test the Gate driver functionality by monitoring the 2 outputs in accordance to 2 provided input signals.
  The 15V supply voltage is provided through the X6 connector via a ribbon cable assembly. In addition, it is required to short the VS node to GND_DIG1 potential.

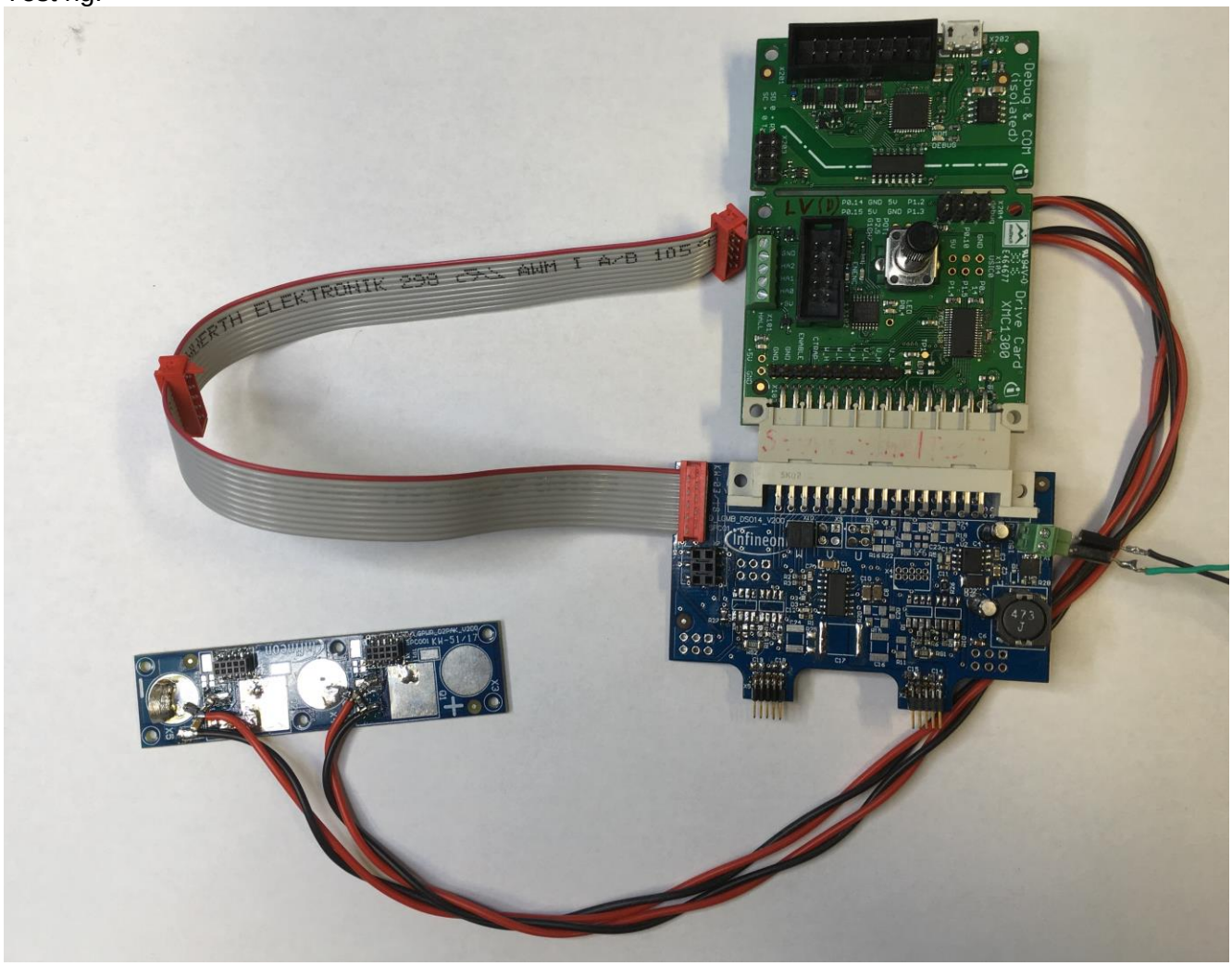
**Table 3 System inputs**

| Signal | Connection point | State | Value (tolerance) |
|---|---|---|---|
| V_15V | X6 (pins 2 and 4) | Active | 15V (±0.1V) |
| GND (reference) | X6 (pins 1 and 3)<br>or<br>PWR board assembly | GND | |
| VS to GND connection | X5 (pin9) to X5 (pin3) | Short | - |
| GD_HIN | X6 (pin 8) | High | 5V (±0.1V) |
| | | Low | 0V (±0.1V) |
| GD_LIN | X6 (pin 7) | High | 5V (±0.1V) |
| | | Low | 0V (±0.1V) |

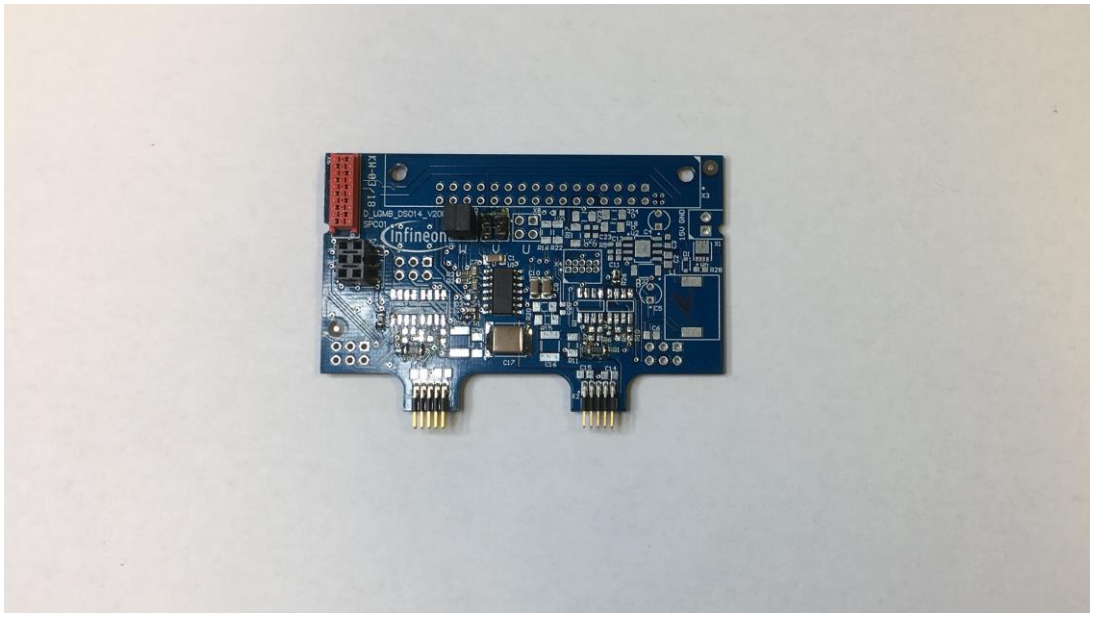
**Table 4 Measured Values (vs. GND)**

| Signal | Connection point | Dependency | Acceptance Criteria |
|---|---|---|---|
| GD_HO | X2 (pin 1 and 2) | GD_HIN – High | 15V (±3V) |
| | | GD_HIN – Low | 0V (±1.5V) |
| GD_LO | X5 (pin 1 and 2) | GD_LIN – High | 15V (±1.5V) |
| | | GD_LIN – Low | 0V (±1.5V) |

Test rig:

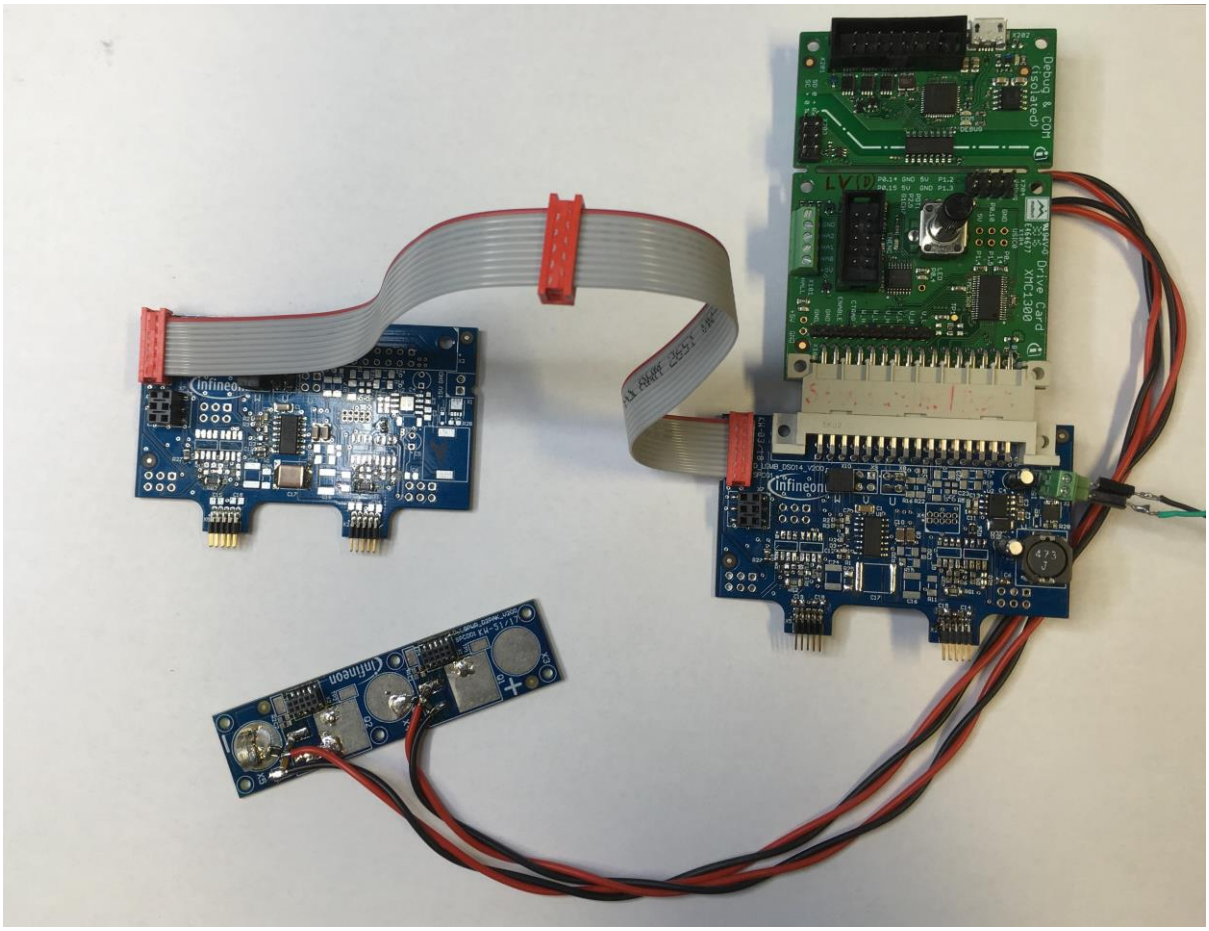



Device under test:

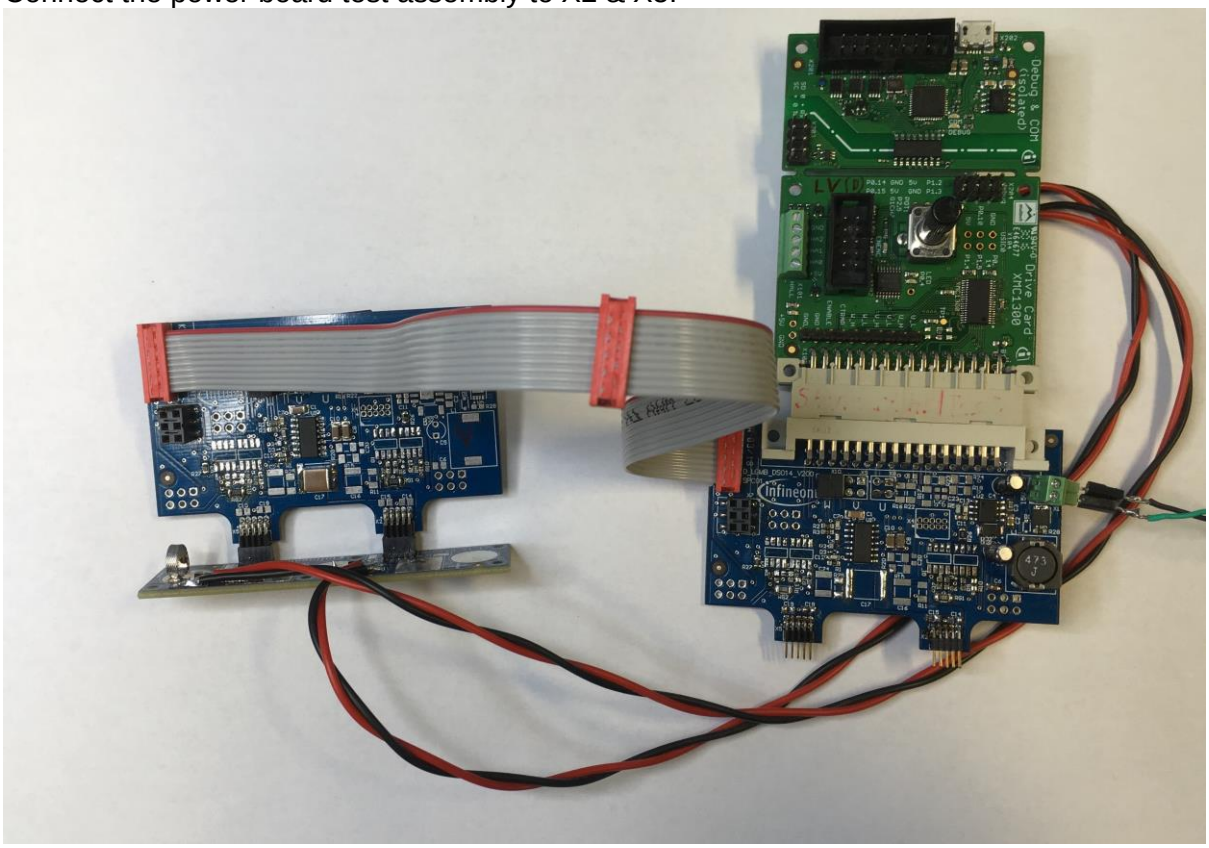


Test procedure:

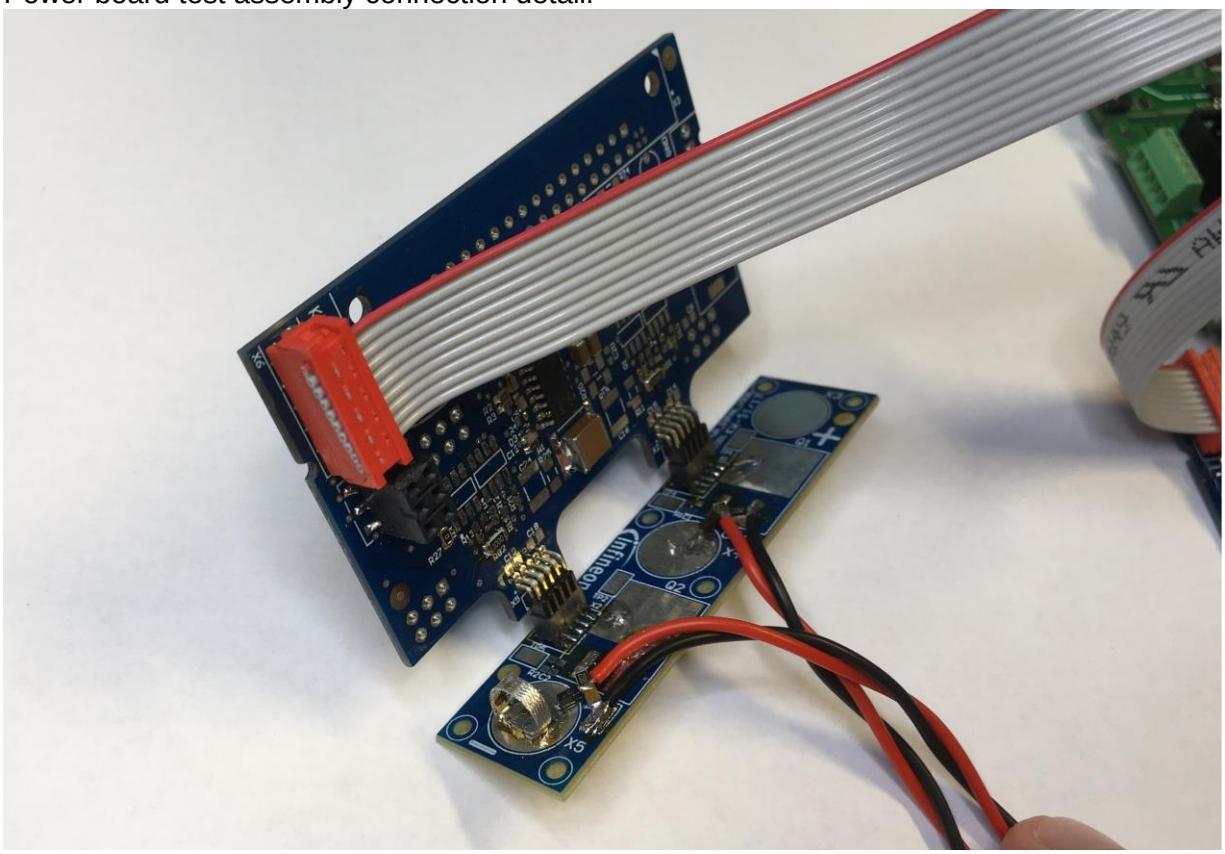
- Connect the counter connector to X6:



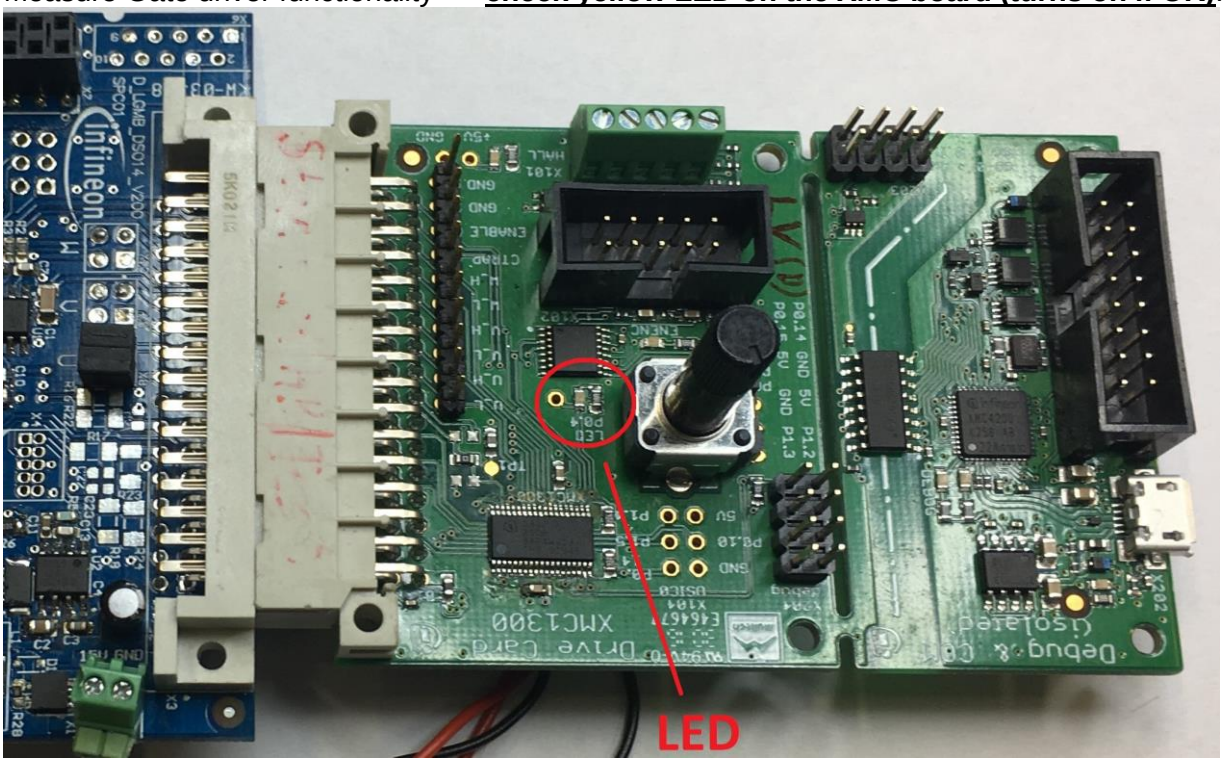
- Connect the power board test assembly to X2 & X5:



- Power board test assembly connection detail:



- Measure Gate driver functionality => **check yellow LED on the XMC board (turns on if OK)**:




**or**:
- Measure GD_HO and GD_LO @ input state 1 (GD_HIN = LOW, GD_LIN = HIGH)
- Change input state 1 >> 2)
- Measure GD_HO and GD_LO @ input state 2 (GD_HIN = HIGH, GD_LIN = LOW)

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Published by
Infineon Technologies AG

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